# DDR 3 Verification IP

## Product Brief

| iUVM Family | Applications |
|---|---|
| 1. DDR3 Memory VIP<br>2. DDR4 Memory VIP | 1. System-on-Chip designs using DDR3 Memory<br>2. Test full timing or bus functional models<br>3. Standalone DDR3 memory and/or memory controller |

## DDR3 VIP Features

**General**

- Compliant with JEDEC DDR3 standard JESD79-3C
- Supports all DDR3 memories
- Advanced System Verilog features like constrained random testing
- UVM Compliant
- Check for DDR3 compliance
- Support full timing models or bus functional models
- Integrates easily with any verification environment
- Perform block level or system level verification

**Monitor, Checker and Scoreboard**

- Monitor DDR3 behavior continuously during simulation
- Assertions based Checker performs protocol checking and compliance for commands and timing
- Scoreboard keeps and reports compliance results
- Detailed log files and error generation
- Detailed Functional Coverage Reports
- Configurable initialization procedure, number of banks, ranks, data and data strobe bus widths, burst lengths, RAS and CAS latencies.
- Elaborate set of callbacks
- Transaction level debugging available
- Rich set of test cases

| Solution | Benefits |
|---|---|
| • Encrypted System Verilog code<br>• Complete verification environment<br>• User Manual and Application Notes | • Quickly check DDR3 for compliance<br>• Detailed reports<br>• Use for block level or system level tests |

### Innovaide's DDR3 VIP Solution

Innovaide provides a comprehensive intelligent solution for DDR3 verification and compliance checking. The solution leverages UVM methodology and verification techniques to quickly check for DDR3 protocol compliance for DDR3 implementations.

### Configurability

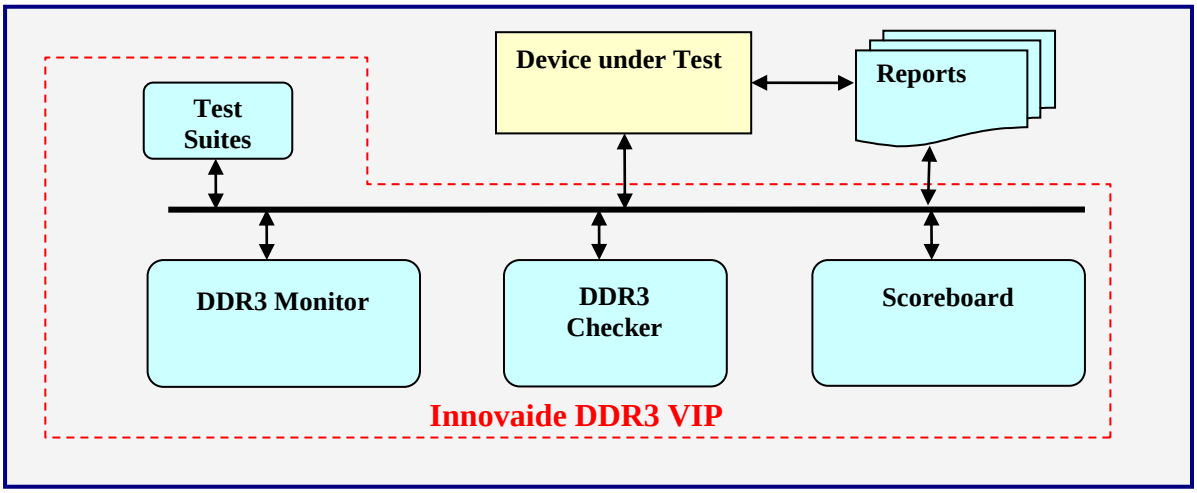
Innovaide provides a highly configurable solution that can be configured at functionality level as well as at feature level.

### Flexible Solution

Innovaide provides a flexible solution that can be used in SoC, ASIC or FPGA simulations. The solution is designed for quick integration into existing verification environment.

## Innovaide DDR3 VIP Application Example

The following diagram shows the application in a typical verification environment




## Innovaide DDR3 VIP Deliverables

**Verification IP**

- Encrypted System Verilog models
- Test Cases and Scripts
- User Manual and Release Notes
- Application Notes and White Papers

**Service and Support**

- Annual support and maintenance
- On-site training and knowledge transfer
- Customization services

Innovaide's highly experienced team will ensure a seemless integration and hand-off of VIP into your verification methodology and environment.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